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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,237	04/20/2004	Tetsuji Togawa	2004_0624	2525
513	7590	11/02/2005	EXAMINER	
WENDEROTH, LIND & PONACK, L.L.P. 2033 K STREET N. W. SUITE 800 WASHINGTON, DC 20006-1021			GEORGE, PATRICIA ANN	
		ART UNIT		PAPER NUMBER
		1765		

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/827,237	TOGAWA ET AL.	
	Examiner	Art Unit	
	Patricia A. George	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 20 April 2004.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-29 is/are pending in the application.
 4a) Of the above claim(s) 1-8 is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 9-29 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date 4/20/04.
- 4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

DETAILED ACTION

Amendments

Amendments to claims were received, on 20 April 2004, and acknowledged.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 10-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oishi et al. of US 5,665,954 in view of Kitano et al. of US 5,944,894.

Oishi et al. discloses a method for CMP conventionally used in semiconductor manufacturing processes (col.1, l.15-16), which provides a CMP apparatus (col.1, l.15-16). Oishi teaches it is conventional to place the polishing apparatus in a room of lower cleanliness than a normal clean room (col.1, l.48-49), but goes on to teach an improvement that reduces manufacturing cost incurred to transport and clean wafers upon returning to the clean room, prior to continue processing (col.1, l.58-62). Oishi teaches it is not preferred to perform the polishing in a separate area from the clean room, as this placement causes a substantial hindrance and the flow of manufacturing

stagnates (col.1, l.54-57). In figure 7, Oishi illustrates the CMP method is performed inside an apparatus that is air tight (col. 8, l.28), by means of outer wall (92) and door (93) which demonstrates isolation from the external environment a closed space that is defined by an enclosing structure of said manufacturing apparatus, and the processing of semiconductor wafers within said closed space by operating a processing device, as in claim 9. Oishi points to maintaining a clean atmosphere within said closed space by operating a purifying system by teaching use of filters, such as HEPA or ULPA (col8, l.39) to clean recirculated air (col.8, 36-38).

Oishi does not discloses maintaining an internal pressure of said closed space to be higher than a pressure in said external environment by operating a pressure elevating device.

Kitano et al. teaches a method used to set and control internal process environment conditions, such as: air speed, air flow, internal pressure, and air cleanliness to a preferable value (col.6, l29-32), for CMP (col.15, l.40) processing, which exhibits the capability of maintaining an internal pressure of said closed space to be higher than a pressure in said external environment where the operation of a pressure elevating device, also illustrated in figure 4. Kitano goes on to teach how to control the rate at which air is discharged, as illustrated in figure 4, a fan (174) and a HEPA filter (175) in a unit (173) (also see text col.6, l.6-7). Figures 5 and 6 continue to illustrate the air supply system is fitted with a controller (170), which is an air conditioning unit (see the brief description of figure 5). Note reference of prior art in conclusion, towards damper.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the method of CMP, as invented by Oishi et al., to Maintain an internal pressure of the closed space to be higher than the pressure in an external environment by employing a pressure operating device, of Kitano et al., because Kitano teaches when used with CMP there are added benefits such as assisting in the treatment of facility temperature, humidity, and purification, which reduce overall operational costs.

As for claim 10, Oishi et al. illustrates the outer wall (92), of figure 8, as a frame that both holds and protects mechanical parts, which defines a structure comprising a housing.

As for claim 11, Oishi et al.'s figure 8 also shows a purifying system comprises a clean unit (95) mounted on the structure (92), and supplies clean air (col.8, l.30) by means of a filter, as discussed above.

As for claim 12, the discussion to claim 1 for prior art regarding the internal pressure and control of the rate discharged.

As to claims 13, 14, and 15, Oishi et al. discloses polishing a semiconductor wafer with a polishing device (as to claim 13), and cleaning the polished wafer (as to claim 14), in the abstract of US 5,665,954. Oishi displays a loader/unloader suction of the CMP apparatus in figure 2, part 26 (as in claim 15). As to the controlling an internal pressure of the individual sections (as in claims 14 and 15) to be higher than an internal pressure of said polishing section, see discussion above towards pressure set to

preferred value. Also see column 8, lines 46-49 for Oishi et al.'s teachings on pressure of compartments individually controlled.

As to claim 16, Oishi et al. teaches the hand-off of the wafer from the polisher to the cleaner via a robot used only for transfer of wet wafers (col.3-4, l.65-1). The doors between sections are shown in Oishi's figure 2, handling robots in figures 3).

As to claim 17, 20, and 21, see discussions above on controlling an internal pressure of the individual sections and pressure of compartments individually controlled.

As to claim 18, see Oishi's teaching in column 3, lines 54-61, for transfer of wafer to polisher, from loader.

As to claim 19, Oishi teaches cleaning and drying occurs in a cleaning section (figure 2 and col.4, lines 7).

As to claims 22-29 see discussions above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: United States Patent 5392845, Air-conditioning device, discloses it is well known that such units control air flow via use of a damper. United States Patent 5,401,212 discloses environmental control systems for modular isolation of semiconductor apparatus, located outside of clean rooms.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patty George whose telephone number is (571)272-5955. The examiner can normally be reached on weekdays between 7:00am and 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Patricia A George
Examiner
Art Unit 1765

PAG
10/05

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER

